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BALANCING VOLTAGE IN MODULAR MULTILEVEL CONVERTER WITH NEAREST LEVEL CONTROL TECHNIQUE AND ASYMMETRIC MULTI-LEVEL INVERTER TOPOLOGY

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Abstract: This paper proposes an asymmetric source configuration of multilevel inverter (MLI) topology with Nearest Level Control (NLC) technique for efficient and cost-effective power conversion. The proposed topology consists of eight unidirectional switches, two bidirectional switches, and four isolated DC sources, producing 25-level and 21-level outputs with 1:5 and 1:4 source configurations, respectively. By using NLC technique for switching control, the topology produces both positive and negative voltage levels without the need for a separate backend H-bridge. Moreover, only four switches are in an ON mode in every state, resulting in less per unit Total Standing Voltage and reduced semiconductor device costs.
High-switching frequency Pulse Width Modulation (PWM) techniques often lead to switching losses in high-level inverters. Therefore, this paper proposes the use of NLC technique to reduce switching losses, making it particularly suitable for high-level inverters. The proposed topology has potential applications in renewable energy integration to the grid and drives application. Simulation results obtained using MATLAB/Simulink validate the proposed topology and demonstrate that the inrush current at the input of DC sources has been eliminated.

Keywords: Asymmetric source configuration, multilevel inverter, Nearest Level Control, switching losses, renewable energy integration, simulation.

Introduction:

Multilevel inverters (MLIs) play a significant role in various power conversion applications such as renewable energy integration, motor drives, and power distribution systems. One of the main advantages of MLIs is their ability to produce high-quality output voltage with fewer harmonic distortions. However, the main challenge in the design of MLIs is the requirement of a large number of isolated DC sources and switches, resulting in high cost and complexity.
Several topologies have been proposed to reduce the number of isolated DC sources and switches, such as Cascaded H-Bridge (CHB), Diode-Clamped (DC), and Flying Capacitor (FC) topologies. Among these topologies, the CHB topology is widely used due to its ability to produce a high number of output voltage levels with fewer semiconductor devices. However, the main disadvantage of the CHB topology is its requirement for a large number of isolated DC sources.
To address this issue, this paper proposes an asymmetric source configuration of MLI topology with NLC technique to reduce the number of isolated DC sources and switches, resulting in a cost-effective and efficient

power conversion system. The proposed topology produces both positive and negative voltage levels without the need for a separate backend H-bridge.

The NLC technique controls the switching of the proposed topology and reduces switching losses, making it particularly suitable for high-level inverters. The proposed topology has potential applications in renewable energy integration to the grid and drives application. Simulation results obtained using MATLAB/Simulink validate the proposed topology and demonstrate that the inrush current at the input of DC sources has been eliminated.

Proposed Asymmetrical MLI Topology

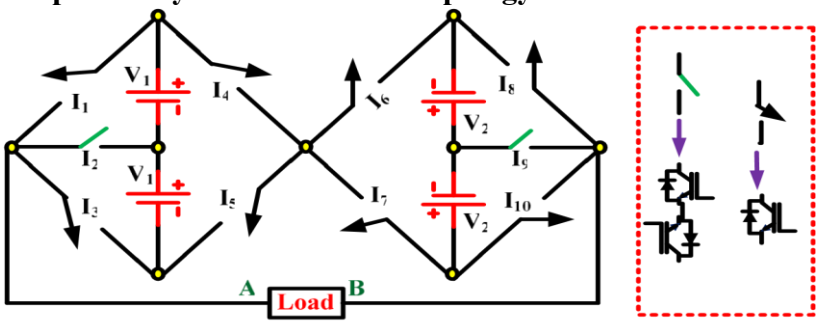

Figure 1. Proposed Asymmetrical MLI topology

The proposed asymmetrical MLI topology is shown in Figure 1. The proposed circuit consists of eight uni-directional switches and two bi-directional switches with four DC sources. With source configuration of 1:5, the peak voltage obtained as $+12V_{dc}$ and with source configuration of 1:4, the peak voltage obtained is $+10V_{dc}$. The switching table for all the voltage levels is shown in Table 1.

The proposed topology is simulated in MATLAB/SIMULINK platform and 25-level output has been generated with 1:5 source configuration. Similarly, using the source configuration as 1:4 with same switching action, the 21-level output can be generated. To generate peak output voltage of $+12V_{dc}$ in 1:5 source configuration topology (i.e $V_1 = V_{dc}$ and $V_2 = 5V_1$) the switches I_1, I_5, I_7, I_8 are turned ON and remaining switches are OFF, which includes all the DC sources. Similarly, to generate the voltage level of $+6V_{dc}$ in 1:5 source configuration topology (i.e $V_1 = V_{dc}$ and $V_2 = 5V_1$) the switches I_2, I_5, I_7, I_9 are turned ON and remaining switches are OFF, which includes only two DC sources. The entire switching action is shown in Table 1, which includes all the voltage levels positive and negative levels from $+12V_{DC}$ to $-12V_{DC}$.

Table 1. Switching Table 1:5 source configuration

S. No	ON State Switches	Output Voltage
1	$I_2 - I_5 - I_7 - I_{10}$	$1V_{dc}$
2	$I_1 - I_5 - I_7 - I_{10}$	$2\ V_{dc}$
3	$I_3 - I_4 - I_7 - I_9$	$3\ V_{dc}$
4	$I_2 - I_4 - I_7 - I_9$	$4\ V_{dc}$
5	$I_1 - I_4 - I_7 - I_9$	$5\ V_{dc}$
6	$I_2 - I_5 - I_7 - I_9$	$6\ V_{dc}$
7	$I_1 - I_5 - I_7 - I_9$	$7\ V_{dc}$
8	$I_3 - I_4 - I_7 - I_8$	$8\ V_{dc}$
9	$I_2 - I_4 - I_7 - I_8$	$9\ V_{dc}$
10	$I_1 - I_4 - I_7 - I_8$	$10\ V_{dc}$
11	$I_2 - I_5 - I_7 - I_8$	$11\ V_{dc}$
12	$I_1 - I_5 - I_7 - I_8$	$12\ V_{dc}$
13	$I_1 - I_4 - I_6 - I_8$	$0\ V_{dc}$
14	$I_2 - I_4 - I_6 - I_8$	$-1\ V_{dc}$
15	$I_3 - I_4 - I_6 - I_8$	$-2\ V_{dc}$
16	$I_1 - I_5 - I_6 - I_9$	$-3\ V_{dc}$
17	$I_2 - I_5 - I_6 - I_9$	$-4\ V_{dc}$
18	$I_1 - I_4 - I_6 - I_9$	$-5\ V_{dc}$
19	$I_2 - I_4 - I_6 - I_9$	$-6\ V_{dc}$
20	$I_3 - I_4 - I_6 - I_9$	$-7\ V_{dc}$
21	$I_1 - I_5 - I_6 - I_{10}$	$-8\ V_{dc}$
22	$I_2 - I_5 - I_6 - I_{10}$	$-9\ V_{dc}$
23	$I_1 - I_4 - I_6 - I_{10}$	$-10\ V_{dc}$
24	$I_2 - I_4 - I_6 - I_{10}$	$-11\ V_{dc}$
25	$I_3 - I_4 - I_6 - I_{10}$	$-12\ V_{dc}$

NLC scheme

Generally, in any inverter the control scheme plays a vital role and these schemes control the gating signals of the switches. In this paper, the technique called Nearest level Control technique (NLC) is used to generate an output voltage of 25-levels. The scheme is explained with the control diagram and waveform synthesis shown in Figure 2. From the control diagram, it is clear that the reference signal V_{ref} (Sinusoidal) is given to the gain block of the value $V_{dc.}$ The ratio V_{ref} / V_{dc} is given to the round function which determines the nearest voltage level from which the switching logic of the inverter is derived and given as gating signals to switches. A nearest level control technique is one of important technique preferably used for high level inverters. If the NLC technique is used for low level inverters then it generates lower order harmonics which are quite difficult to eliminate. The waveform synthesis proves that the reference voltage cuts exactly at the midpoint of the staircase waveform as the round$_{0.5}$ {} function is applied.

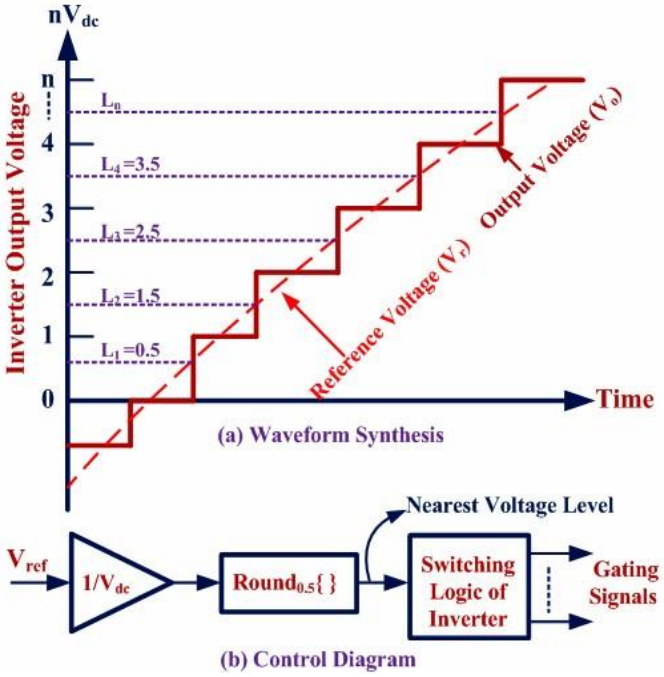

Figure 2. NLC Scheme

Simulation Results

Figure 3 shows the inverter input DC source currents with 1:5 source configuration. The peak value of the current is reduced suddenly if the modulation index is shifted at 0.06s. It is clear from the figure 3 that there are no huge inrush currents at the input of the inverter. Figure 4 shows the inverter output voltage and current. The generated 25- level output with peak value as 12V_{dc} (with V_{dc} = 20V) = 240V is shown in figure 4. After the modulation index has been shifted from 1 to 0.4 the inverter generates 11level output with peak value as 5V_{dc} = 100V. The peak inverter output current at modulation index as unity is 2.398 A and at 0.06s the peak value has been reduced to 0.9953 A. The voltage and current stresses of all switches for 1:5 source configuration is shown in figure 5. The 21-level output voltage of the inverter with 1:4 source configuration is shown in figure 6. The peak voltage value of the inverter is +10 V_{dc} = 200V at modulation index as unity. The output levels of the same inverter configuration are reduced to 9 levels at 0.06s when the modulation index is shifted to 0.4 from unity. Now, the peak voltage value of the inverter is +4V_{dc} = 80 V. Similarly, by referring to the inverter output current waveform from the figure 6, the peak value of the current before 0.06s is 1.996A and after 0.06s the peak current is reduced to 0.7986 A as modulation index is reduced to 0.4. The Simulation parameters are given in Table 3.

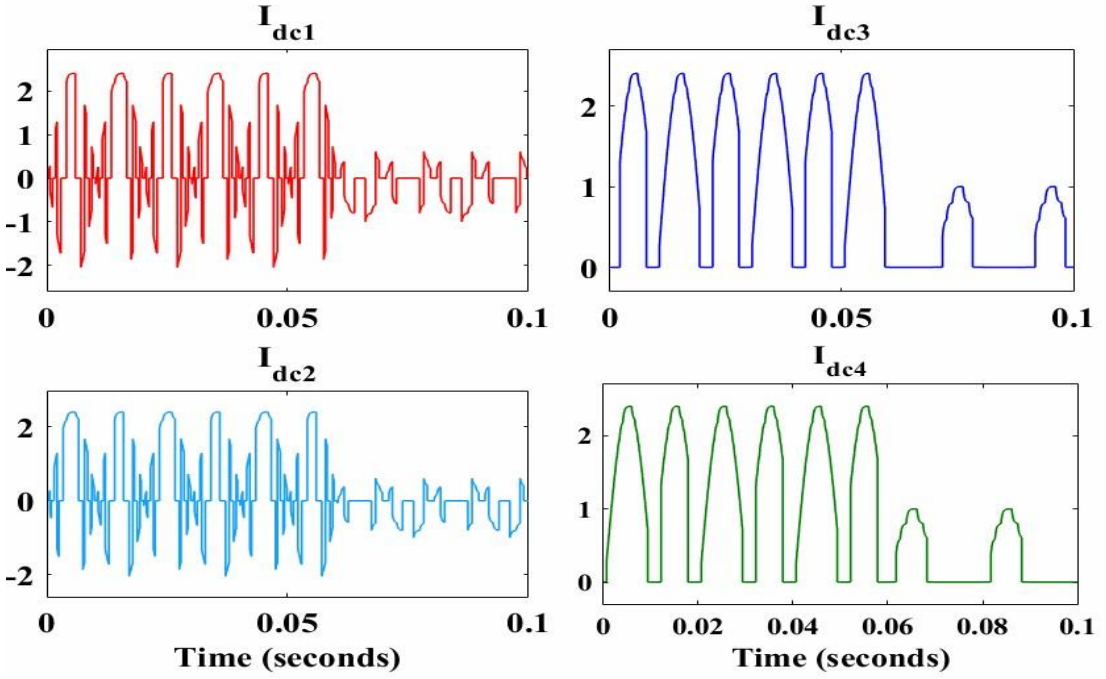

Figure 3. Inverter Input DC source currents for 1:5 source configuration with modulation index shifted from 1 to 0.4 at 0.06s

The Comparison of different asymmetrical MLI topologies is shown in Table 2, where 'p' indicates, number of levels. In Hosseinzadeh et al. (2012), the number of IGBTs required is $10\log_{17}^{p}$ where 'p' is considered as 17 levels only. The harmonic analysis is shown in figure 7, here at the fundamental frequency the inverter peak output voltage is 240.6V and %THD is 3.26% then it finally meets the IEEE1547 standards

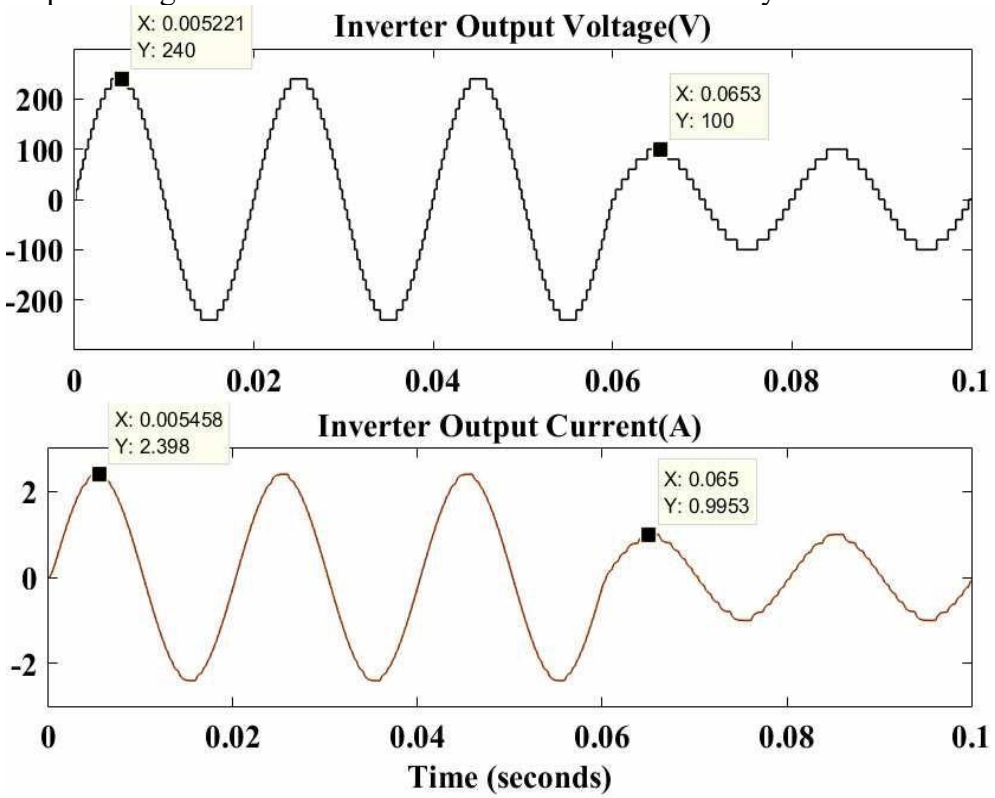

Figure 4. Inverter Output voltage and Inverter output current for 1:5 source configuration with modulation index shifted from 1 to 0.4 at 0.06s

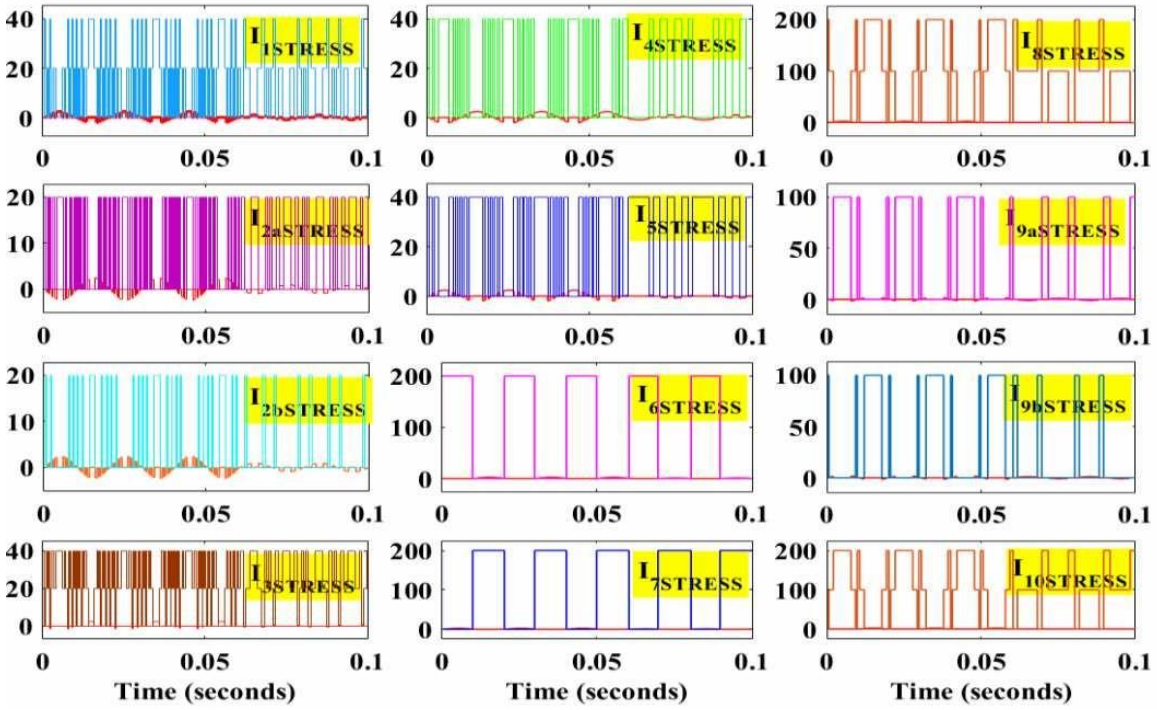

Figure 5. Voltage and current stresses of all power semiconductor switches for 1:5 source configuration.

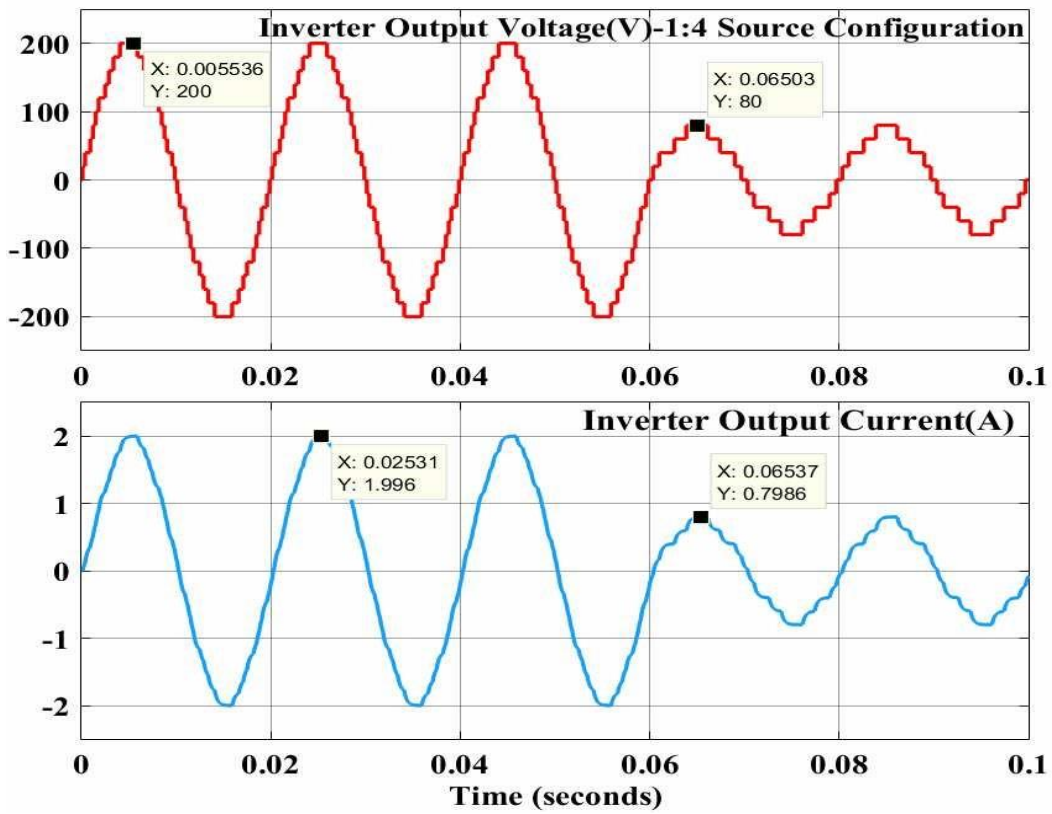

Figure 6. Inverter output voltage and Inverter output current for 1:4 source configuration with modulation index shifted from 1 to 0.4 at 0.06sec

Table 2. Comparison of different asymmetrical MLI topologies: Generalized Equations

Topologies	N_{IGBT}	N_{Driver}	$N_{sources}$	TSV*(V_{DC})	Negative Levels
Ebrahimi et al. (2012)	$8\log_5^P$	$6\log_5^P$	$2\log_5^P$	2.75(P-1)	With H-Bridge
Khosroshahi (2014)	$3\log_2^{P+1}+1$	$2(\log_2^{P+1}+1)$	$\log_2^{P+1}-1$	3.667(P-1)	With H-Bridge
Babaei et al. (2015)	$5\log_2^{P+5}$-9	$5\log_2^{P+5}$-9	$3\log_2^{P+5}$-8	(3.5P-4.5)	With H-Bridge
Babaei et al. (2014)	$4\left(\log_3^{\left(p+\frac{1}{2}\right)}+1\right)$	$4\left(\log_3^{\left(p+\frac{1}{2}\right)}+1\right)$	$2\log_3^{\left(p+\frac{1}{2}\right)}$	3(P-1)	With H-Bridge
Babaei (2008)	$6\log_3^{\left(p+\frac{1}{2}\right)}+4$	$3\log_3^{\left(p+\frac{1}{2}\right)}+4$	$2\log_3^{\left(p+\frac{1}{2}\right)}$	4.5(P-1)	With H-Bridge
Gupta and Jain (2014)	$\sqrt{4P-3}+1$	$\sqrt{4P-3}+1$	$0.5\left(\sqrt{4P-3}-1\right)$	2(P-1)	Inherent
Alishah et al. (2017)	$10\log_{17}^P$	$8\log_{17}^P$	$4\log_{17}^P$	2.5(P-1)	With H-Bridge
Hosseinzadeh et al. (2012)	$10\log_{17}^P$	$8\log_{17}^P$	$4\log_{17}^P$	2.5(P-1)	With H-Bridge
Sharma and Kapoor (2016)	$10\log_{17}^P$	$8\log_{17}^P$	$4\log_{17}^P$	2.5(P-1)	With H-Bridge
Proposed	$5\log_5^P$	$5\log_5^P$	$2\log_5^P$	2.5(P-1)	Inherent

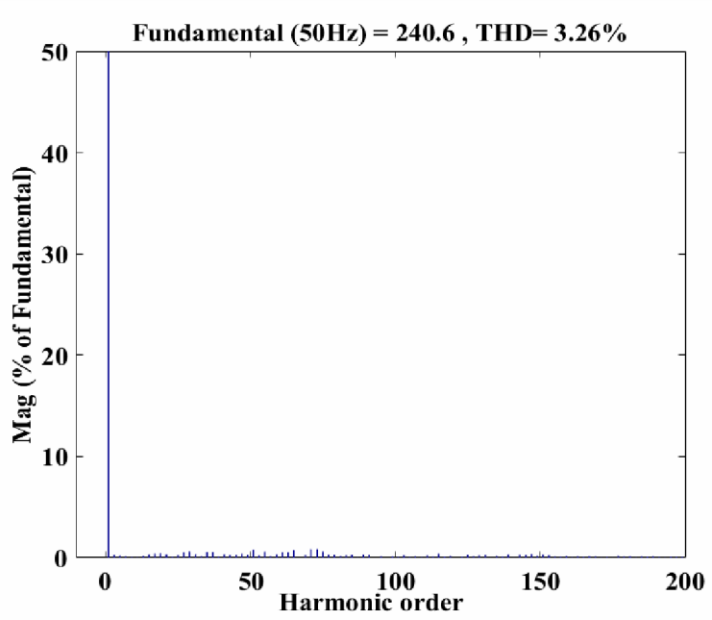

Figure 7. Harmonic Spectrum of Inverter Output Voltage-25 level output with 1:5 Source Configuration**:** MI=1.0

Table 3. Simulation Parameters

S. No	Description	Value
1	V_{DC}	20V
2	R	100 ohms
3	L	30mH
4	Output Frequency	50Hz
5	Voltage gain	1.0

6	**Source Configurations**	**1:5 and 1:4**
7	**Modulation Index**	**1 to 0.4**
8	**TSV (p.u)**	**5.0**

Conclusion

In this paper, a new asymmetrical MLI topology with two types of source configurations has been proposed and which requires less switch count when compared with other conventional topologies. The cost requirement of the switching devices can become reduces since less per unit TSV value is obtained. Basically, the reduction of switch count indicates that the respective reduction in gate drive circuits, heat sink and protection circuits. The NLC technique is used to provide the gate pulses to the switches which reduces switching losses and %THD value greatly reduces as compared with other conventional PWM control techniques. The change in peak value of the inverter output voltage and output current is observed with the step change of modulation index values from 1 to 0.4. The %THD value obtained for 25-level inverter output voltage with 1:5 source configuration is 3.26% and finally it meets the requirement of IEEE standards. The drawback of this topology is that it does not provide any boosting ability since voltage gain as unity. This topology is well suitable for grid connected applications.

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